IN THE CLAIMS:

Please cancel claims 27-29 without prejudice.

Please amend claims 1, 7, 8, 14, 15, 19, and 20, and add new claims 30-34 as follows:

1. (Amended) An integrated circuit having a plurality of active components including junctions formed in a monocrystalline substrate doped locally, and at least one passive component situated above the active components, said integrated circuit comprising:

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a first insulating layer separating the active components and a base of the passive component; and

a metal terminal for electrically connecting the passive component with at least one of the active components, the metal terminal being formed in the thickness of the first insulating layer and having a lower surface that contacts a junction of the one active component such that the lower surface of the metal terminal extends over a boundary of the junction of the one active component.

7. (Amended) An integrated circuit including a plurality of transistors, a plurality of passive components, and a level of local metal connections formed within a first insulating layer that is deposited on top of the transistors of the integrated circuit, said integrated circuit comprising:

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a first metal terminal passing completely through the thickness of the first insulating layer, the first metal terminal constituting a first stage of contact between an active area of the integrated circuit and a first level of interconnection;

a second metal terminal passing completely through the thickness of the first insulating layer, the second metal terminal vertically connecting an active area of the integrated circuit to a passive component that directly contacts the upper surface of the first insulating layer; and

a third metal terminal passing completely through the thickness of the first insulating layer, the third metal terminal horizontally connecting two separate active areas of the integrated circuit.

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8. (Amended) The integrated circuit according to claim 7, wherein the second metal terminal has a lower surface that contacts a junction of one of the transistors of the integrated circuit such that the lower surface of the metal terminal extends over a boundary of the junction of the one transistor.

14. (Amended) An integrated circuit comprising:

an onboard memory plane of DRAM cells in a matrix, each of the cells including a control transistor and a storage capacitor;

a plurality of MOS transistors;

a first level of interconnection above the storage capacitors;

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a first insulating layer separating the MOS transistors and the base of the storage capacitors; and

a level of local connections including three metal terminals each opening onto each side of the first insulating layer,

wherein the first metal terminal forms a first stage of contact between one active area of the integrated circuit and the first level of interconnection,

the second metal terminal vertically connects one active area of the integrated circuit with one plate of one of the storage capacitors, the one plate of the one storage capacitor directly contacting the upper surface of the first insulating layer, and

the third metal terminal horizontally connects two separate active areas of the integrated circuit.

15. (Amended) The integrated circuit according to claim 14, wherein the second metal terminal has a lower surface that contacts a junction of the one active area such that the lower surface of the metal terminal extends over a boundary of the junction of the one active area.

19. (Amended) An information processing system including at least one integrated circuit, the integrated circuit comprising:

an onboard memory plane of DRAM cells in a matrix, each of the cells including a control transistor and a storage capacitor;

a plurality of MOS transistors;

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a first level of interconnection above the storage capacitors;

a first insulating layer separating the MOS transistors and the base of the storage capacitors; and

a level of local connections including three metal terminals each opening onto each side of the first insulating layer,

wherein the first metal terminal forms a first stage of contact between one active area of the integrated circuit and the first level of interconnection,

the second metal terminal vertically connects one active area of the integrated circuit with one plate of one of the storage capacitors, the one plate of the one storage capacitor directly contacting the upper surface of the first insulating layer, and

the third metal terminal horizontally connects two separate active areas of the integrated circuit.

20. (Amended) The information processing system according to claim 19, wherein the second metal terminal has a lower surface that contacts a junction of the one active area such that the lower surface of the metal terminal extends over a boundary of the junction of the one active area.

Please add new claims 30-34 as follows:

--30. (New) The integrated circuit according to claim 1, wherein the first insulating layer is a

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single layer and the only insulating layer provided between the active components and the base of the passive component.--

--31. (New) The integrated circuit according to claim 1, wherein the base of the passive component directly contacts the upper surface of the first insulating layer.--

--32. (New) The integrated circuit according to claim 1, further comprising:

areas of dielectric material for separating active areas that contain the active components of the integrated circuit,

B5 wherein part of the lower surface of the metal terminal contacts one of the areas of dielectric material.--

--33. (New) The integrated circuit according to claim 7, wherein the first insulating layer is a single layer and the only insulating layer provided between the transistors and a base of the passive component.--

--34. (New) The integrated circuit according to claim 7, wherein the third metal terminal is a local horizontal interconnection that directly connects two separate active areas of the integrated circuit.--